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EXAMINER	
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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAMESH V. PERI, JOHN S. FERNANDO,
RAVI KOLAGOTLA, and
SRINIVAS P. DODDAPANENI

Appeal 2008-0264
Application 10/717,085
Technology Center 2100

Decided: April 28, 2008

Before JAMES D. THOMAS, JOSEPH L. DIXON,
and THU ANN DANG, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1 through 28. We have jurisdiction under 35 U.S.C. § 6(b).

Since independent clam 1 is the best, most succinct representation of the disclosed and claimed invention, it is reproduced below:

1. A method comprising:

implementing read accesses to the same portion of a memory line in the same cycle.

The following reference is relied on by the Examiner:

Kawasaki US 5,742,790 Apr. 21, 1998

Claims 1 through 28 stand rejected under 35 U.S.C. § 102(a) as anticipated by or, in the alternative, under 35 U.S.C. § 103 as obvious over Kawasaki.

Rather than repeat the positions verbatim of Appellants and the Examiner, reference is made to the Brief and Reply Brief for Appellants' positions, and to the Answer for the Examiner's positions.

OPINION

As expanded upon here, we sustain the rejections of claims 1 through 28 under both statutory provisions with which they are rejected as set forth by the Examiner in the Answer.[1] In accordance with Appellants' statements at page 12 of the principal Brief on appeal, independent claim 1 is considered to be representative of all claims on appeal, since no arguments are presented in the Brief and Reply Brief as to any other claims.

Although it appears that the Examiner's statement of the rejection at page 3 of the Answer as well as the responsive arguments at page 4 of the Answer could have been better developed, the evidence of anticipation and/or obviousness provided by Kawasaki leads us to conclude the subject

[1] Since the Examiner's reference to the Johnson's patent at the bottom of page 3 of the Answer is stated to be not cited as the basis of the rejection of the present claims on appeal, we have not considered it in our deliberations.

matter of representative independent claim 1 on appeal is anticipated and/or otherwise would have been obvious under the noted statutes.

The discussion at column 1, lines 19 through 23 of Kawasaki sets forth the context of the disclosure involving a super scaler type of processor that utilizes two or more arithmetic units and a multi-port cache memory in order to provide simultaneous processing of a plurality of instructions. This context is further amplified in the summary paragraph bridging columns 3 and 4 which also indicates that the data processing environment is of a parallel processor approach. The continued use of the word WAY throughout the disclosure of Kawasaki is initially defined in the discussion at column 1, lines 35 through 38 such as to indicate that the so-called WAY or WAY number corresponds to the number of different methods to divide a storage region of a memory. The discussion associated with prior art figure 4 indicates that four WAYs or portions of a memory may be accessed. Significantly, as relied upon by the Examiner at the bottom of page 4 of the Answer, the discussion in the last paragraph at column 1, indicates that such a load-load command from the plural processor environment noted earlier is a type of simultaneous access at the same address. It is not disputed in the Brief and Reply Brief that this involves a read-read simultaneous read command.

The various figures as well as the summary of the invention at column 2, lines 19 through 36 indicate that an AND gate provides a compare circuit capability for comparing the so-called set address signals and the so-called SAME WAY HIT signal so as to send a control signal to the cache memory for informing whether the signals are identical and simultaneously accessed

or not. (Similar AND logic is used by Appellants in their disclosed figure 2.) Therefore, the artisan would well appreciate in addition to the showings in various figures that the terminology of identical and simultaneous access signal generation is referred to as the SAME ADDRESS throughout the reference.

Of most significance in the descriptive portion of Kawasaki patent is the statement at column 3, lines 26 through 28 that states the "SAME WAY HIT signal is a signal to indicate that the signal is accessing the same WAY as another signal on another part of the cache is accessing" (emphasis added).

From the above teachings, we strongly agree with the Examiner's view that the subject matter of representative method independent claim 1 of implementing plural read accesses to the same "portion" of a memory line occurs in the "same cycle."

We are unpersuasived by Appellants' remarks principally set forth in the Reply Brief that seem to take the position at the bottom of page 1 of this Brief that the reference only deals with the detection and does not really address what happens if there is a simultaneous access. This view belies an artisans' perspective of the teachings of Kawasaki.

Moreover, Appellants' assertions in terms of their own logical conclusion regarding the suggestibility of the reference expressed in the first paragraph at the top of page 2 of the Reply Brief is merely attorney's speculation and also does not come to grips with the teaching value of Kawasaki from an artisan's perspective. We totally disagree with the understanding that Appellants conclude or otherwise presume that when

simultaneous storage commands are received, it would be necessary to execute one before the other. Such is clearly not the case in the plural, parallel processor environment in Kawasaki. Appellants have not argued before us that the operations in Kawasaki do not occur within the same cycle as claimed. Therefore, Appellants have waived any arguments as to this feature of representative independent claim 1 on appeal.

Since the weight of the arguments and evidence provided by the Examiner of unpatentability under 35 U.S.C. § 102 and 35 U.S.C. § 103 supports the Examiner's position, we conclude that the Appellants have not shown any error in the Examiner's view as to the unpatentability of all claims on appeal. Therefore, the decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a). See 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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